METHOD FOR MANUFACTURING WAFER LEVEL CHIP SCALE PACKAGE STRUCTURE

DESCRIPTION

BACKGROUND OF THE INVENTION

[Para 1] Field of Invention

[Para 2] The present invention relates to a chip package structure and a method for manufacturing the chip package structure. More particularly, the present invention relates to a method for manufacturing a wafer level chip scale package structure with a compact size.

[Para 3] Description of Related Art

[Para 4] Chip scale package (CSP) is a package that has an area of no more 20% larger than that of the die. With better protection by molding encapsulation and better board level reliability, CSP prevails over the direct chip attach (DCA) and chip on board (COB) technologies.

[Para 5] Taking chip scale packaging process as an example, the backs of the chips are attached to the substrate and the chips are electrically connected to the substrate through wire bonding. The chips and the substrate are simultaneously encapsulated by the encapsulating material in transfer molding process. After performing singulation by dicing, a plurality of chip package structures is obtained. Figures 1 is a cross-sectional view of the prior art CSP structure after dicing. Referring to Figures 1, one chip package structure 102 includes the substrate 110, the chip (die) 130 and the molding compound 170. In general, the back of chip 130 is glued onto the substrate 110 by silver epoxy, and the chip (from the top surface) is electrically connected to the substrate 110 through wires 180 by wire bonding. The chip 130 and wires 180

are covered by the molding compound 170 formed by encapsulation. The substrate 110 further includes solder balls 190 on the bottom for external electrical connection. Due to the application of wires and the molding compound, the package structure is somehow larger and thicker than the chip itself. In general, the size (area) of CSP package is about 20% larger than the die and the height (thickness) of CSP package is around 1.2 mm.

[Para 6] However, issues around the reliability of the packaging still remain. For the package structure comprised of silicon chip, bismaleimide triazine (BT) substrate, the molding compound and silver epoxy, it would encounter various stress-related problems due to different coefficient of thermal expansion (CTE). For the prior art CSP structure, the CTE mismatch between the package substrate and the silicon chip is large (about 14 ppm) thus lowering the reliability and quality of the package structure. Moreover, the fabrication processes of the prior art CSP structure are complex and the widely used BT substrate is quite costly.

SUMMARY OF THE INVENTION

[Para 7] The present invention provides a chip package structure with a compact size and lower costs and a method for manufacturing the chip package structure.

[Para 8] The present invention provides a method for manufacturing a wafer level chip scale package structure, which increases reliability of the attachment between the chip and the substrate.

[Para 9] As embodied and broadly described herein, the present invention provides a method for manufacturing a wafer level chip scale package structure including the following steps. After providing a glass substrate and a wafer comprising a plurality of chips, the active surface of the wafer is connected to the top surface of the glass substrate. The wafer is connected with the glass substrate through either bumps or pads thereon. After drilling the glass substrate to form a plurality of through holes, a plating

process is performed to form a plurality of via plugs in the through holes. Afterwards, a singulation step is performed and a plurality of chip scale package structures is obtained.

[Para 10] According to one embodiment, the bumps on the active surface of the wafer are bonded to the top surface of the glass substrate by eutectic bonding or anisotropic conductive film (ACF). According to another embodiment, pads on the active surface of the wafer are attached to the top surface of the glass substrate by thermal cured adhesives.

[Para 11] According to the present invention, the size ratio of die (chip) and the CSP package structure is nearly 1.0 and is more compact than the prior art package structure. Due to the lower cost of the glass substrate and less area required for the glass substrate, the cost for the package structure of this invention is estimated to be much lower than that of the conventional package structure. Moreover, the manufacturing processes provided in the present invention are greatly simplified without wire bonding or encapsulation process, which reduce the package costs and increase the package yield.

[Para 12] Besides, by using the glass substrate, the thermal stress due to CTE mismatch between the chip and the substrate is reduced and the reliability of the package structure is improved.

[Para 13] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[Para 14] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[Para 15] Figure 1 is a cross-sectional view of the prior art CSP package structure after dicing.

[Para 16] Figs. 2-7 are cross-sectional views illustrating the manufacturing steps of the CSP package structure according to one preferred embodiment of the present invention.

[Para 17] Figs. 8-12 are cross-sectional views illustrating the manufacturing steps of the CSP package structure according to another preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[Para 18] In semiconductor packaging, faster and smaller electronic packaging approaches with high I/O counts and complex semiconductor devices are intensely required. Flip chip (FC) and wafer level chip scale packaging (WL-CSP) meet the requirements of high I/O-devices and even for low pin-count applications. In addition, wafer level packaging can reduce the cost of packaging each individual chip.

[Para 19] Figs. 2-7 are cross-sectional views illustrating the manufacturing steps of a CSP structure according to one preferred embodiment of the present invention.

[Para 20] Referring to Figure 2, a semiconductor wafer 230 is provided with an active surface 232 and an opposite back surface 234. A plurality of bonding pads 236 are disposed on the active surface 232 of the wafer 230 and a plurality of bumps 238 are disposed on the bonding pads 236. According to the preferred embodiment, bumps 238, such as, Sn/Pb solder bumps, gold bumps or other high melting point bumps, are formed over the bonding pads 236. In addition, an under metal metallurgy (UBM) layer (not shown) is formed for increasing attachment between the bonding pad 236 and the bump 238, which is made of metals selected from the following group consisting of nickel, gold, titanium, copper and palladium.

[Para 21] The bumps 238 are formed by, for example, implanting globular tin/lead globes onto the surface of the bonding pad 236. Alternatively, the bumps 238 are formed by, for example, stencil printing the low melting temperature tin/lead paste to the surface of the bonding pad 236 and performing a reflow step to obtain the globular bumps. Alternatively, the bump 238 can be formed by electroplating method.

[Para 22] Referring to Figure 3, a substrate 210 is provided with a top surface 212 and a back surface 214. The substrate 210 is, for example, an indium tin oxide (ITO) conductive glass plate provided with a metallic interconnect pattern 216 on the top surface 212. The thickness of substrate 210, for example, is about 100-400 microns, preferably 200-300 microns. The wafer 230 is flipped, so that the active surface 232 faces the top surface 212 of the substrate 210. The flipped wafer 230 is then arranged onto the substrate 210, so as to bond the bumps 238 of the wafer 230 onto the top surface 212 of the substrate 210. The bumps 238 can be bonded to the interconnection pattern 216 of the substrate 210, by either eutectic bonding or using anisotropic conductive film (ACF). The eutectic bonding metallurgically attaches the bumps of the wafer to the substrate by using eutectic preforms in various compositions. Alternatively, the ACF consisting of non-filled adhesive layer and a thermal-setting adhesive layer filled with conductive particles can be placed between the bumps and the substrate for bonding. Still, the bonding should create uniform connection between the bumps 238 of the wafer 230 and the substrate 210. The wafer 230 is electrically connected to the substrate 210 through the bumps 238 and the interconnection pattern 216.

[Para 23] By using a glass substrate, the CTE mismatch between the wafer (or die) and the glass substrate is relatively small, so that thermal stress caused by CTE mismatch is greatly reduced. In accordance with the embodiment, no underfill process is required.

[Para 24] Referring to Figure 4, a wafer dicing process is performed to cut the wafer 230 into a plurality of dies 231 by using wafer saw technology. Basically, the wafer is cut along the scribe-lines.

[Para 25] Referring to Figure 5, a through-hole (TH) drilling process is performed by, for example, laser drilling, to form through-holes 240 through the substrate plate 210. The size of the through-holes can be about 20-50 microns. Afterwards, a plating process, for example, electroplating or electroless plating process, is performed to fill up the through-holes 240, so that metal vias 242, for example, copper vias, are formed within the through-holes.

[Para 26] Alternatively, the process steps described in Figures 4 and 5 can be performed in a reverse order, i.e. firstly performing the TH drilling process and the plating process, and subsequently performing the wafer dicing process. In this case, the through-holes (or vias) are aligned with the scribe-lines of the wafer 210.

[Para 27] Optionally, a wafer testing process can be performed to test electrical properties of the CSP package structure or the die by probing through the vias 242.

[Para 28] Referring to Figure 6, a singulation (dicing) process is performed to dice the glass substrate 210 (and the interconnection pattern 216 on the substrate) through the metal vias 242, so that the WL-CSP package structure 200 are divided into a plurality of individual CSP package structures 202. Each CSP package structure 202 includes at least a portion of the substrate 210 (with a portion of the interconnection pattern), the die 231 connected to the substrate through a plurality of bumps 238, and a plurality of vias 242, arranged as described above and shown in Fig. 6. The size ratio of die 231 and the obtained CSP package structure 202 is nearly 1.0.

[Para 29] The obtained CSP package structure 202, as shown in Fig. 6, can be directly applied as a peripheral type package structure.

[Para 30] However, if the CSP package structure 202 will be applied as an array type package structure, the glass substrate 210 needs to be pre-treated to form a redistribution layer 218 on the back surface 214 for the following ball implanting process. The redistribution layer 218 can be formed by, for example, sputtering an ITO film or electroplating a copper film on the back surface 214 of the glass substrate 210. Moreover, additional process needs to

be performed to the array type CSP package structure. Referring to Figure 7, a plurality of solder balls 220 are formed on the redistribution layer 218 of the substrate 210 by solder-ball attachment.

[Para 31] In the above embodiment, the dicing process is performed prior to the formation of solder balls. Alternatively, it is possible to form solder balls before the singulation process.

[Para 32] Figs. 8-12 are cross-sectional views illustrating the manufacturing steps of a CSP structure according to another preferred embodiment of the present invention.

[Para 33] Referring to Figure 8, a semiconductor wafer 830 is provided with an active surface 832 and an opposite back surface 834. A plurality of pads 836, for example, contact pads, are disposed on the active surface 832 of the wafer 830. The pads 836 are designed to partially extend to cover scribe-lines 838 of the wafer 830. The scribe-line 838 usually has a width of about 80-150 microns.

[Para 34] Referring to Figure 9, a substrate 810 is provided with a top surface 812 and a back surface 814. The thickness of substrate 810, for example, is about 100-400 microns, preferably 200-300 microns. The wafer 830 is flipped, so that the active surface 832 faces the top surface 812 of the substrate 810. The flipped wafer 830 is then arranged onto the substrate 810, so as to attach the pads 836 of the wafer 830 onto the top surface 812 of the substrate 810. The pads 836 can be attached to the substrate 810, by thermal cured adhesives 816. Optionally, the back surface 834 of the wafer 830 can be ground by backgrinding technology to a predetermined thickness, for example, as thin as about 25-50 microns.

[Para 35] Alternatively, as shown in Fig. 9A, to the back surface 834 of the wafer 830, an etching process is performed to remove the scribe-lines 838, until surfaces of the pads 836 are exposed. In this case, the wafer 830 has in fact been cut into individual dies.

[Para 36] By using a glass substrate, the CTE mismatch between the wafer (or die) and the glass substrate is relatively small, so that thermal stress caused by

CTE mismatch is greatly reduced. In accordance with the embodiment, no underfill process is required.

[Para 37] Following the process steps described in Figs. 9 and 9A and referring to Figs. 10 and 10A respectively, a through-hole (TH) drilling process is performed by, for example, laser drilling, to form through-holes 840 through the substrate plate 810. The size of the through-holes can be about 20-50 microns. Afterwards, a plating process, for example, electroplating or electroless plating process, is performed to fill up the through-holes 840, so that metal vias 842, for example, copper vias, are formed within the through-holes 840. In general, the locations of the vias 842 (or through-holes 840) are aligned with the pads 836. Preferably, each of the vias 842 is aligned to and connected to one pad 836.

[Para 38] Optionally, a wafer testing process can be performed to test electrical properties of the CSP package structure or the die by probing through the vias 842 or even through the exposed pads 836 (Fig. 9A).

[Para 39] Referring to Figures 11, a singulation (dicing) process is performed to cut the wafer 830 into a plurality of dies 831 and dice the glass substrate 810 (and the thermal cured adhesive 816 on the substrate) through the metal vias 842, so that the WL-CSP package structure 800 are divided into a plurality of individual CSP package structures 802. For the structure shown in Figure 9A, the wafer 830 has already been cut into individual dies by removing the scribe-lines, the singulation process dices up the substrate 810 to obtain individual CSP package structures 802. Each CSP package structure 802 includes at least a portion of the substrate 810, the die 831 connected to the substrate through a plurality of pads 836, and a plurality of vias 842, arranged as described above and shown in Fig. 11. The size ratio of die 831 and the obtained CSP package structure 802 is nearly 1.0.

[Para 40] The obtained CSP package structure 802, as shown in Fig. 11, can be directly applied as a peripheral type package structure.

[Para 41] However, if the CSP package structure 802 will be applied as an array type package structure, the glass substrate 810 needs to be pre-treated to form a redistribution layer 818 on the back surface 814 for the following

ball implanting process. The redistribution layer 818 can be formed by, for example, sputtering an ITO film or electroplating a copper film on the back surface 814 of the glass substrate 810. Moreover, additional process needs to be performed to the array type CSP package structure. Referring to Figure 12, a plurality of solder balls 820 are formed on the redistribution layer 818 of the substrate 810 by solder-ball implantation.

[Para 42] In the above embodiment, the dicing process is performed prior to the formation of solder balls. Alternatively, it is possible to form solder balls before the singulation process.

[Para 43] According to the present invention, the size ratio of die (chip) and the singulated CSP package structure is nearly 1.0. Compared with the prior CSP package, the package structure of this invention has a size about 20% less. Moreover, without the wires and the molding compound, the package structure of this invention has a height (thickness) of about 300-800 microns. Therefore, the package structure of this invention is more compact than the prior art structure.

[Para 44] On the other hand, the manufacturing processes provided in the present invention are greatly simplified without wire bonding or encapsulation process, which reduce the package costs and increase the package yield. Because the cost of the glass substrate is lower than the conventional BT substrate, the cost of the resultant package is also reduced. The cost for the package structure of this invention is estimated to be about 40-50% lower than that of the conventional package structure.

[Para 45] Moreover, by using the glass substrate, the thermal stress due to CTE mismatch between the chip and the substrate is reduced and the reliability of the package structure is improved.

[Para 46] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.